CLAIMS

1. A semiconductor device comprising a semiconductor substrate having therein a low-capacitance substrate region, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, characterized in that:

a plurality of substrate openings are formed in said low-capacitance substrate region, penetrating at least an undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate.

2. The semiconductor device according to claim 1, wherein a low-permittivity insulating material is embedded in said substrate openings.

3. The semiconductor device according to claim 1 or 2, wherein a length of said substrate openings within said semiconductor substrate is equal to or larger than half a thickness of said semiconductor substrate, or said substrate opening penetrate said semiconductor substrate.

4. The semiconductor device according to any one of claims 1 to 3, wherein said substrate openings are randomly arranged as viewed normal to a surface of said substrate.

5. The semiconductor device according to any one of claims 1 to 3, wherein said substrate openings are formed so that no linear current path is formed crossing said low-permittivity substrate region as viewed normal to a surface of said substrate.

6. The semiconductor device according to any one of claims 1 to 5, wherein a high-permeability region is provided to overlie said low-permittivity substrate region, said high-permeability region including a high-permeability material embedded in an interlevel dielectric film.

7. The semiconductor device according to claim 6, wherein said high-permeability region includes therein a plurality of high-permeability magnetic rods arranged and including said high-permeability material having an electric conductivity and embedded in respective film openings having an aspect ratio (ratio of depth to diameter or a side) of 1 or above, said film openings penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

8. The semiconductor device according to claim 6, wherein said high-permeability region includes therein a plurality of high-permeability magnetic rods arranged and including said high-permeability material having an insulating property and embedded in respective film openings, said film openings penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

9. A semiconductor device comprising a semiconductor substrate, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein a high-permeability region is provided in an interlevel dielectric film, characterized in that:

said high-permeability region includes therein a plurality of high-permeability magnetic rods including a high-permeability material having an electric conductivity and embedded in respective

film openings, said film openings having an aspect ratio (depth/diameter or a side) of 1 or above and penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

10. A semiconductor device comprising a semiconductor substrate having therein a low-capacitance substrate region, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein a high-permeability region is provided in said interlevel dielectric film, characterized in that:

said high-permeability region includes a plurality of high-permeability magnetic rods including a high-permeability material having an insulating property and embedded in respective film openings, said film openings penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

11. The semiconductor device according to any one of claims 6 to 10, wherein said high-permeability material is a composite material including a low-permittivity insulating material and a high-permeability magnetic material including an electric conductivity or an insulating property.

12. The semiconductor device according to claim 11, wherein said low-permittivity insulating material is a porous insulating material.

13. The semiconductor device according to claim 7 or 9, wherein said high-permeability magnetic rods include a high-permeability material film coating an inner wall surface of said

insulating film openings and a low-permittivity insulating material embedded inside said high-permeability material film.

14. The semiconductor device according to any one of claims 7 to 13, wherein said high-permeability region includes a high-permeability magnetic plane overlying and/or underlying said high-permeability magnetic rods, said high-permeability magnetic plane having a material including a high-permeability material embedded in depressions formed in a surface of said interlevel dielectric film.

15. The semiconductor device according to any one of claims 1 to 14, wherein an inductor is formed to overlie said low-permittivity substrate region or said high-permeability region.

16. The semiconductor device according to any one of claims 1 to 15, wherein an analog circuit is formed on said semiconductor substrate in said low-capacitance substrate region or an area including said high-permeability region.

17. The semiconductor device according to any one of claims 1 to 16, wherein a logic circuit is formed on said semiconductor substrate in an area other than an area in which said low-capacitance substrate region or said high-permeability region is formed.

18. The semiconductor device according to any one of claims 1 to 4, wherein an on-chip antenna interconnect is formed on said low-capacitance substrate.

19. The semiconductor device according to claim 18, wherein said on-chip antenna interconnect is formed in a peripheral area of a semiconductor chip.

20. The semiconductor device according to claim 18, wherein said on-chip antenna interconnect is formed in an I-character, L-character or U-character shape or in multiple loops.

21. The semiconductor device according to any one of claims 18 to 20, wherein said on-chip antenna interconnect is configured by interconnect layers embedded in slit-like openings which are formed to penetrate a plurality of said interlevel dielectric films.

22. The semiconductor device according to any one of claims 19 to 21, wherein a grounded shield interconnect is formed inside said on-chip antenna interconnect.

23. The semiconductor device according to claim 22, wherein said shield interconnect is configured by interconnect layers embedded in slit-like openings formed to penetrate a plurality of said interlevel dielectric films.

24. A method for manufacturing a semiconductor device including a semiconductor substrate, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein a high-permeability region is provided in said interlevel dielectric film, said method comprising the consecutive steps of:

(1) forming the transistor on said semiconductor substrate;

(2) forming a plurality of substrate openings penetrating at least undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate;

(3) embedding an insulating material in said openings; and

(4) grinding a bottom surface of said semiconductor substrate.

25. The method according to claim 24, wherein said insulating material embedded in said step (3) is low-permittivity insulating material having a lower permittivity than silicon oxide.

26. The method according to claim 24 or 25, further comprising, between said step (1) and said step (2), the additional step of forming an interlevel dielectric film covering said transistor on said semiconductor substrate.

27. The semiconductor device according to any one of claims 1 to 23, wherein an interconnect configured by a plurality of interconnect layers is provided in said low-capacitance substrate region.

28. The semiconductor device according to claim 27, wherein said interconnect layers configure an inductor.

29. The semiconductor device according to claim 27 or 28, wherein interconnects in said plurality of interconnect layers are connected electrically in parallel through a plurality of via-plugs.

30. The semiconductor device according to claim 27 or 28, wherein ends of interconnects in said plurality of interconnect layers are connected together through a plurality of via-plugs so that said

plurality of interconnect layers are connected electrically in series.

31. The semiconductor device according to claim 30, wherein a current flowing through first interconnects formed in a first interlevel dielectric film and a current flowing through second interconnects formed in a second interlevel dielectric film adjacent to said first interlevel dielectric film do not flow opposite to each other.

32. The semiconductor device according to claim 30, wherein a first interconnect layer formed in a first interlevel dielectric film and a second interconnect layer formed in a second interlevel dielectric adjacent to said first interlevel dielectric film conduct currents in the same direction in the structure wherein said plurality of interconnect layers are connected in series.

33. The semiconductor device according to claim 30, wherein interconnects of a first interconnect layer formed in a first interlevel dielectric film and interconnects of a second interconnect layer formed in a second interlevel dielectric film adjacent to said first interlevel dielectric film do not extend overlapping each other as viewed in the vertical direction in the structure wherein said plurality of interconnect layers are connected in series.

34. The semiconductor device according to any one of claims 1 to 23 and 27 to 33, wherein contact plugs configuring electrodes of said transistor and an insulating film containing at least silicon are formed on a first interlevel dielectric film in said low-permittivity substrate region, said insulting film having constituent atoms and composition different from those of said first interlevel dielectric film.

35. The semiconductor device according to any one of claims 1 to 23 and 27 to 34, wherein an insulating containing at least silicon is formed in said low-permittivity substrate region on a first interlevel dielectric film receiving therein contact plugs configuring electrodes of said transistor, said insulating film having constituent atoms and composition difference from those of said first interlevel dielectric film.

36. The semiconductor device according to any one of claims 1 to 23, and 27 to 35, wherein said low-permittivity insulator rods have a topmost surface located lower than a topmost surface of contact plugs in said low-capacitance substrate region.

37. The semiconductor device according to any one of claims 1 to 23 and 27 to 36, wherein an insulating film is disposed to cover said low-permittivity insulator rods, said insulating film having a higher permittivity and higher mechanical strength than an insulating film embedded in said rods.